

• fR MEM_SRAM

Embedded memories are the most critical blocks concerning permanent and transient faults such soft-errors. Fault detection in memories is typically addressed by using Error Detection and Correction Codes (EDC or ECC) but several limitations are inherently embedded in EDC/ECC. In accordance with IEC61508, the standard EDC/ECC itself is not allowing SIL3 compliance for a memory sub-system composed by the memory array, the memory controller and the protection circuitry; EDC/ECC has a meaningful impact in terms of area and timing overhead; for large memories, multiple faults cause protection degradation; from a system point of view, EDC/ECC is not a solution for faults caused by unintentional or malicious accesses.

fR MEM_SRAM is a fault supervisor IP for SRAM-based memory sub-systems. On top of EDC/ECC, fR MEM_SRAM provides a set of proprietary techniques to fulfil the limitations of a pure EDC/ECC based solution. Area overhead is tuneable with the "Two Memories Architecture" [TMA], allowing a flexible partitioning of data in pages with selectable protection levels. Timing overhead introduced by EDC/ECC is prevented by the "Fast-Track" or "Latency Hiding" techniques, enabling the highest operating frequency with no modification either to the CPU logic or to the memory controller. The "Scrubbing" technique, a low-power background running task scanning the memory, maintains the protection level decreasing the Failure In Time [FIT] by catching silent faults. The "Distributed MPU" provides a local memory protection tackling HW and SW system-level faults.

fR MEM_SRAM has been verified with YOGITECH fR methodology including a Failure Mode and Effect Analysis [FMEA] and the use of a proprietary fault injector to inject faults at different levels of abstraction.

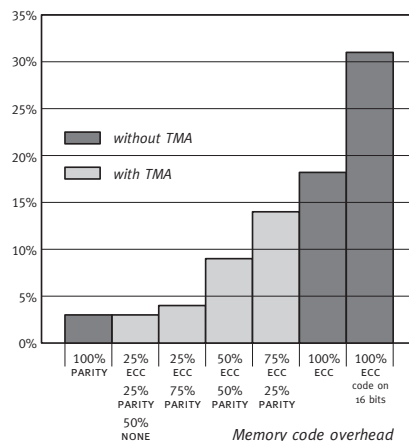
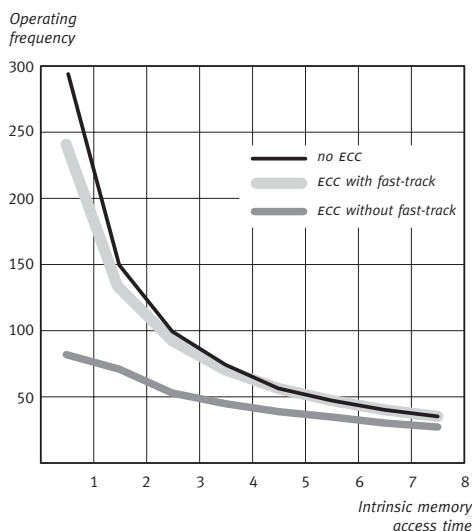
fR MEM_SRAM is certified by TÜV SÜD: it fulfils the safety integrity level SIL3 in accordance with IEC61508, the international norm for safety critical electronics.

fR MEM_SRAM is part of YOGITECH faultRobust technology and it can be connected through the dedicated fR NET bus to other fR IPs in order to implement a full soc robustness.

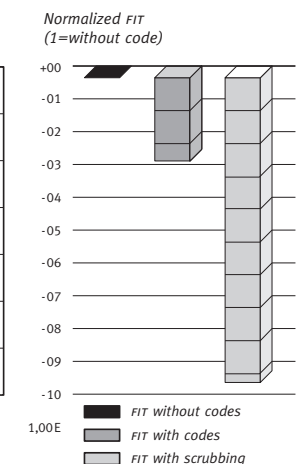
YOGITECH's faultRobust

is the technology for addressing and achieving fault robustness in Integrated Circuits. It provides a set of IPs, tools and methodologies for the detection and correction of faults affecting the different parts of the electronic equipment or soc. Each fR IP can be stand-alone, protecting a particular component such as CPU, memory system and peripherals, or it can be combined with other fR IPs for a complete solution.

YOGITECH's faultRobust technology optimizes costs by minimizing gate count, software overhead and power consumption; it reduces the common mode effects by adding diversity; it minimizes performance impact; offering a platform-based modular and reusable approach; it increases diagnostic capability; and it addresses the emerging norm IEC 61508, thus providing guidelines and a methodology for a system to be IEC 61508 adherent.



Graphs for a 128KBytes SRAM with optimized SEC-DED code, 32 bit data, 7 bits of code, addresses included in code, artisan CMOS 0.18 LowLeakage, Worst Automotive conditions, scrubbing of the full memory each 12 hours, SER of 0.001 FIT/bit.



• fR MEM_SRAM

ARCHITECTURE

fR MEM_SRAM is composed of two blocks to be connected to the memory and to the memory controller. The Fault Protection Memory Manager [F-MEM] block includes all the options related to coding/decoding and other special techniques such *Fast-Track* and *Scrubbing*. The Memory Controller Extension [MCE] block extends the memory controller and it manages the way the bus interacts with the fR MEM_SRAM, being responsible of functions such read-modify-write, *Distributed MPU* technique and so on. *Distributed MPU* can be used to divide the memory in pages each one with attributes, permissions and fault protection types.

USAGE

The two blocks of fR MEM_SRAM are designed to wrap the memory system without modifications to the memory controller and without interfering with third-parties Built-In-Self-Test [BIST] or Built-In-Self-Repair [BISR] units. The fR MEM_SRAM can be ordered in one of the many possible configurations depending on the selection of the following options:

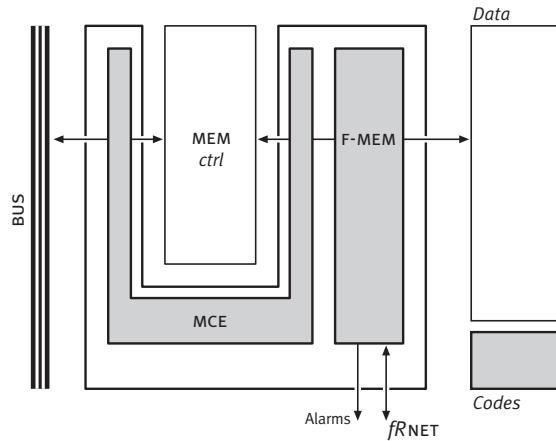
- Coding schemes (*Parity*, *HAMMING*, *Optimized BCH*) with any coding width
- Addresses included in the code or not
- Read-modify-write functionality (for byte/half-word access)
- Different coding/decoding architectures (with reuse, pipelined)
- Errors logging: error counters with programmable thresholds
- Memory controller interfaces: *AMBA*, *8051*, *native* (e.g. *TCM*)
- fRNET to connect fR MEM_SRAM to other fRIPS

Special option (proprietary techniques):

- “Fast-Track” (“lite” or “full”)
- Configurable latency with “Latency-Hiding”
- “Scrubbing”, (“scrub&repair” and “auto-scrub”)
- “Two-memories / Banked Two-Memories” [TMA/BTMA] architectures
- “Distributed MPU”

fR MEM_SRAM is delivered with a verification plan to check its integration in the memory sub-system and an RTL out-of-the-box integration testbench that tests the main functionalities of the fR MEM_SRAM. It can also be used as a template for top-level verification.

BLOCK DIAGRAM



MAIN FEATURES

- Memory code overhead from 5% to 50% as a function of coding scheme and use of the TMA/BTMA architectures.
- Negligible access time overhead with the *Fast-Track* or *Latency Hiding* technique.
- Failure In Time [FIT] decrease factor from 10^3 to 10^9 as a function of coding scheme and use of the *Scrubbing* technique.
- Gate count between 1K and 10K gates depending on the configuration.
- $\geq 99\%$ test coverage, including seamless interface to external BIST.
- $\geq 99\%$ diagnostic coverage (*sil3* as certified by TÜV SÜD).

DELIVERABLES

- RTL description, including top-level integration template for the chosen configuration.
- Functional models for behavioral simulation.
- SPIRIT XML IP description file.
- Verification plan and RTL out-of-the-box testbench.
- Synthesis scripts.
- User Guide, including TÜV SÜD certification report for integration in compliance with IEC 61508
- Online Support Service.
- Training on demand.